REMARKS

This is in response to the Office Action dated November 17, 2004. Claim 10 has been canceled. Thus, claims 1-9 and 11-20 are now pending.

Claims 7, 10 and 20 objected in paragraph 6 of the Office Action. Claim 10 has been canceled. However, the objection as to claims 7 and 20 is respectfully traversed to the extend the Examiner still considers it. In particular, claims 7 and 20 are different since the depend from different independent claims. Because they depend from different independent claims, indirectly, claims 7 and 20 are not duplicates of each other and are entirely proper.

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Admitted Prior Art Figs. 4-5 (APA) in view of Perera. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires "a method of semiconductor device fabrication using a semiconductor substrate comprising a lattice-strain relaxed silicon germanium layer and a lattice strained silicon layer formed in this order on a silicon substrate or on a substrate having a silicon layer on the surface thereof, said method comprising: an etching step comprising etching portions for device isolation regions of said semiconductor substrate so as to form device isolation grooves; a deposition step comprising depositing a silicon film on said semiconductor substrate, including in the device isolation grooves formed in said etching step so that the silicon film contacts sidewalls of at least the lattice-strain relaxed silicon germanium layer and sidewalls of the lattice strained silicon layer at least along side(s) of the grooves; an oxidation step of oxidizing the deposited silicon film; and forming transistors in respective areas between the grooves in and/or over the lattice strained silicon layer." The cited art fails to disclose or suggest the aforesaid underlined aspects of claim 1.

The APA fails to disclose or suggest the deposition of a silicon film in the trench and subsequent oxidation of the same as called for in claim 1. The APA is entirely unrelated to significant aspects of claim 1. Apparently recognizing this deficiency in the APA, the Examiner cites Perera.

Perera discloses in Figs. 4-8 depositing a silicon layer 28 on a substrate over silicon oxide buffer 14 and silicon nitride layer 16. Then, the silicon layer 28 is heat treated using a dry oxidation process to form silicon oxide layer 30 in the trench (e.g., col. 2, lines 45-49 and 57-61). Perera states that this process is used to minimize the formation of voids (e.g., col. 1, lines 51-52; col. 3, lines 39-40). The Examiner contends that it would have been obvious to have used such a silicon layer and subsequent heat treatment described by Perera in the process of the APA in order to minimize the formation of voids.

The Section 103(a) rejection is traversed for at least the following three (3) reasons.

First, one of ordinary skill in the art would have never made the alleged combination of the APA and Perera. The APA relates to a structure where a strain-relaxed SiGe layer and a strained Si cap layer are exposed at sides of a trench region. A *problem arises because the strain relaxed SiGe layer and the strained Si layer have different thermal oxidation rates* from each other (e.g., pg. 3, lines 15-23). The presence of different thermal oxidation rates for these layers causes non-uniformity and hence induces defects thereby causing an increase in leak current if thermal oxidation is used (pg. 3, lines 23-25). Thus, the example problem which may be solved by the invention of claim 1 is specific to the use of a SiGe layer and a Si layer on a substrate which have different thermal oxidation rates if exposed at sides of trenches. On the other hand, this problem is not present in Perera. Perera has no SiGe layer and has no Si layer exposed at sides of trenches. Instead, Perera's trenches expose oxide layer 14 and silicon nitride layer 16 at

sides thereof. The combination of these materials cannot be thermally oxided – thus, the problem realized by the APA is not present in Perera. Importantly, *Perera uses the silicon layer 28 only because nitride layer 16 cannot reasonably be thermally oxided. However, such a nitride layer is not present in the APA.* Thus, because this problem is not present in the APA, one of ordinary skill in the art would never have used Perera's technique in the structure of the APA. Still further, the oxide 14 and nitride 16 layers in Perera are removed and are not even present in the final device – the opposite of what occurs in the APA. Thus, there would have been no reason why one of ordinary skill in the art would have used the silicon layer 28 of Perera in the process of the APA – there simply would have been no need to do so and the cited art lacks any suggestion in this respect.

Second, amended *claim 1 expressly precludes removal of the entire silicon layer before transistors are formed.* In contrast, Perera removes layers 14 and 16 entirely. Again, Perera teaches directly away from the invention of claim 1 in this respect, evidencing the non-obviousness of the claim. Even if one were to have used these layers in the structure of the APA, the invention of amended claim 1 still would not be met.

Third, Perera discloses depositing silicon layer 28, but the silicon layer is deposited on layers of silicon oxide 14 and silicon nitride 16 as shown in Fig. 4. Perera does not have a lattice-strain relaxed silicon germanium layer and a lattice strained silicon layer formed over at least this layer. The only reason why Perera uses his silicon layer is due to the presence of the nitride layer 16, which cannot reasonably be thermally oxided. Since such a nitride layer is not present in the APA, there is no reason why one of ordinary skill in the art would have used the silicon layer of Perera in combination with the structure of the APA.

The Section 103(a) rejection of claim 1 based on Imai in view of Perera is flawed for the same reasons discussed above.

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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